

Signal Integrity & EMC Considerations in PCB Design

(One Day Seminar)

Fundamentals of Signal Integrity

- Transmission Line Equivalent Circuit
- Relative Permittivity (Dielectric Constant)
- Propagation Delay Within Various Materials
- Chart of FR-4 Material
- Ringing and Reflections
- Typical Transmission Line System
- Identification of Signal Distortion
- Crosstalk
- Design Techniques to Prevent Crosstalk
- Power and/or Ground Bounce
- Typical Bounce Waveform
- Component Selection Related to EMC

Fundamentals of EMC

- Component Characteristics at RF Frequencies
- How Printed Circuit Boards Create EMI
- Right Hand Rule
- Maxwell's Equations
- Closed Loop Circuit
- Radiated Emissions from a Closed Loop Circuit
- Loop Area Between Components
- Common-Mode and Differential-Mode Currents
- Basic Concept for EMC Suppression
- Summary of EMI Development Within PCBs

Bypassing and Decoupling

- Defining Capacitor Usage
- Purpose of Using Capacitive Structures
- Capacitors and Resonance
- Using Capacitors in Parallel
- Effects of Capacitors in Parallel
- Power and Ground Plane Capacitance
- Capacitive Loops Created by Decoupling Capacitors
- **Placement Recommendations**

Layer Stackup Assignment

- Single and Double-Sided Recommended Layout
- Multi-Layer Stackup Assignments
- Film and Manufacturing Concerns

Impedance Control and Trace Routing

- Impedance Control Equations
- Capacitive Loading
- Calculating Maximum Trace Length for Trace Routing
- Routing Layers
- Layer Jumping - Use of Vias
- Trace Separation and *the 3-W Rule*
- Guard and Shunt Traces

Terminations (Signal Integrity Concerns)

- Fundamental Concepts of Trace Termination
- Transmission Line Effects
- Termination Methodologies
- Where to Locate Terminators
- What Happens When One Cannot Terminate
- Fundamental Reasons Why EMI is Developed

Crossing the Barrier

- Isolation (Moating), Bridging and Violations

Electrostatic Discharge (ESD Protection)

- Description of an ESD Event
- ESD Waveforms and Triboelectric Series
- Comparison of Various Voltage Levels
- Failure Modes for ESD
- Design Technique for ESD Protection
- Circuit Layout Techniques
- System Level Protection
- Guard Bands