

ConceptHDL Class 16.01

CA Design

1.0 Day 1

1.1 Getting Started

1.1.1 Introduction

1.1.2 Explain Course Objectives:

Hands on class

Learn How to Start a New Project

Learn to use the schematic editor

Learn to use other tools in the workflow

File structure

Create Netlist and BOM

Ask students for other objectives

1.2 Basic Board Design Flow

1.2.1 Objectives:

Open an existing project and view file structure

Create a new project

Exercise project level Concept setup options

Discuss setup for user level and site level customization

1.2.2 Project (directory) Structure (each project in a separate directory)

1.2.3 View an existing project

1.2.4 Examine directory structure and files

1.3 Design Entry and Packaging

Objectives:

Create a two page schematic

Check for errors

Cross reference signal names

Assign refdes manually & automatically

Create netlist reports

Create BOM

1.4 Project Setup

1.4.1 Create a New Project

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- 1.5 Editing a Schematic
 - 1.5.1 Add Component (component browser)
 - 1.5.2 The Standard library
 - 1.5.3 Copy
 - 1.5.4 Attributes
 - 1.5.5 Draw Wire
 - 1.5.6 Signal Names
 - 1.5.7 System-Assigned Signal Names
 - 1.5.8 Synonym
 - 1.5.9 Add pwr & gnd
 - 1.5.10 Write page
 - 1.5.11 Manipulating Pages
- 1.6 Introduction to Packaging
 - What Packaging Does
 - Assigning Reference Designators Manually
 - Automatic Packaging
 - Viewing and Fixing Errors
 - Viewing the Design Directory
 - 1.6.1 Packager Inputs
 - 1.6.2 Explain Logical-to-Physical Assignment
 - 1.6.3 Run the Packager
 - 1.6.4 Packager Outputs
- 1.7 The Packager Reports
 - 1.7.1 Objectives:
 - 1.7.2 Electrical Rules Check
 - 1.7.3 The Reports Utility
 - 1.7.4 Bill of Materials

2.0 Day 2

- 2.1 Cross Referencer
- 2.2 Plotting
- 2.3 Hierarchical Design
 - 2.3.1 Objectives:
 - Create a hierarchical design

- Use top down methodology
- Use bottom up methodology
- Learn more Concept Commands
- Cross reference and plot the design
- 2.3.2 Discuss What is Hierarchical Design?
- 2.3.3 Discuss Naming Issues
- 2.3.4 Components of a Hierarchical Block
- 2.3.5 Review canned hierarchical design
- 2.3.6 Creating a Hierarchical Design
- 2.3.7 Preparing the top down Schematic
- 2.3.8 Exploring Other Commands
- 2.3.9 Working with Groups
- 2.3.10 Preparing the bottom up Schematic
- 2.4 Packaging the Hierarchical Design
- 2.5 Introduction to Board Layout
 - 2.5.1 Discuss Mainstream Board Design
 - 2.5.2 Review Project Directory Structure
 - 2.5.3 Netlist Files
 - 2.5.4 Running Export Physical

3.0 Day 3

- 3.1 Transferring to Allegro
- 3.2 Running Import Physical
- 3.3 Packaging the Design
- 3.4 Hierarchical Connectivity
- 3.5 Hierarchical Cross Referencing and Plotting
- 3.6 PDF Generator
- 3.7 Design Rules
 - 3.7.1 Objectives:
 - Add part properties to control placement
 - Add net properties to control traces
 - Introduce the Constraint Manager
 - 3.7.2 Attaching Allegro Properties
 - 3.7.3 Floor planning

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- 3.7.4 Controlling Part Placement
- 3.7.5 Net_Physical_Type property
- 3.7.6 The Constraint Manager
- 3.7.7 Creating Net Classes in Constraint Manager

4.0 Day 4

- 4.1 Students create new schematic, independently
- 4.2 Creating a Design Variant (optional)
- 4.3 Archiving
- 4.4 Engineering Changes
 - 4.4.1 Objectives:
 - Start a new project from an existing project
 - Modify and repackage the schematic
 - Use design differences to compare the revised schematic to the board layout (optional)
 - 4.4.2 Modify an Existing Project
 - 4.4.3 Importing Designs from Other Projects
 - 4.4.4 Using Export Physical to Implement Changes
 - 4.4.5 Previewing the ECO
 - 4.4.6 Using the Constraint Manager with Allegro
 - 4.4.7 Design Synchronization
- 4.5 Rules Checker
- 4.6 Advanced Use Study
 - 4.6.1 Objectives:
 - Look at real issues that engineers face
 - 4.6.2 Highlighting Critical Components
 - 4.6.3 Highlighting Critical Routing
 - 4.6.4 Cross Probing
 - 4.6.5 Design Rules Summary
- 4.7 Design Reuse (optional)
 - 4.7.1 Design Reuse Flow
 - 4.7.2 Schematic Properties
 - 4.7.3 Packaging for Reuse
 - 4.7.4 Backannotation

4.8 Q & A